IN THE SPECIFICATION:

In Paragraph [0061] beginning at the bottom of page 18:

[0061] In regard to the data communication format according to the present invention, a header of 6 bytes is added to the record controlling data, and the header is stored in a 6 [[bytes]] byte register 431 of the header analyzing block 423 to be analyzed. In regard to the configuration of the header, the first two bytes area channel, the next two bytes are a length and the next two bytes are the data, which is used for negotiation of data communication in order that the interface unit 27 can confirm and determine communication conditions or communication protocol about hardware with the information processing apparatus 200. The channel indicates whether the data following the header is the command or the compressed recording data, and the data from 00H or 02H is the command and the data from 40H is the remote command and the compressed recording data. The upper byte indicates receiving while the lower byte indicates sending. The length is the amount (bytes) of the data included in the header. The command is such controlling command as feeding control, transfer control and discharge control of the recording papers and drive control of the carriage 61 in order to perform recording control in regard to the inkjet type recording apparatus 50.

In Paragraph [0079] beginning at the top of page 28:

[0079] Fig. 10 and Fig. 11 are diagrams schematically showing the state until compressed recording data is hardware-developed in the decoded circuit 28 and

stored in the line buffer 281 in the DECU 41. In addition, [[Fig. 12 is a diagram]] Figures 12A – 12D are diagrams schematically showing the state until the developed recording data is transferred and stored from the line buffer 281 to the local memory 29.

In Paragraph [0088] beginning at the bottom of page 31:

[0088] Continuously, the compressed recording data DMA-transferred from the FIFO memory 425 to the decode circuit 28 is 11H and 02H (Transfer S18). The lower address (even address) of 11H is the data, besides the data of the previous count of FDH. Therefore, 11H is repeatedly developed 3 times [[(257-254=3)]] 257-253=4, and stored in the A face of the line buffer 281, and when the accumulated data in the A face has reached 16 bytes, the remaining data gets sequentially stored in the B face. And, the upper address (odd address) of 02H is the count, and the next data (98H, B0H and F2H) of 3 bytes (2+1=3) is developed as it is without repetition, and sequentially stored in the B face of the line buffer 281 (Transfers S19 to S20.)